

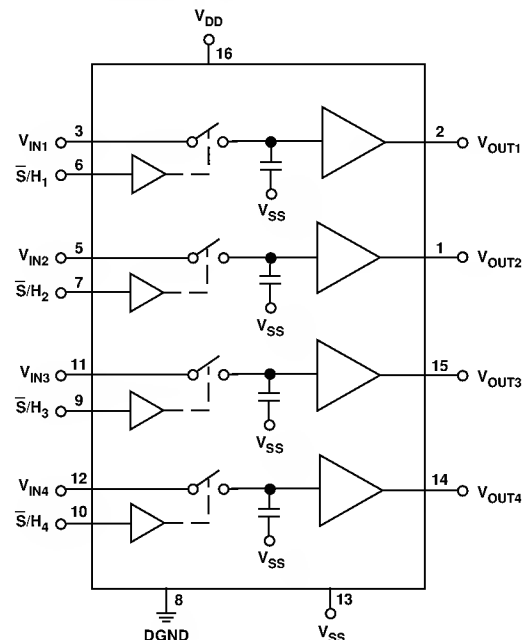
## FEATURES

**Four Independent Sample-and-Holds**  
**Internal Hold Capacitors**  
**High Accuracy: 12 Bit**  
**Very Low Droop Rate (2 mV/s typ)**  
**Output Buffers Stable for  $C_L \leq 500$  pF**  
**TTL/CMOS Compatible Logic Inputs**  
**Single or Dual Supply Applications**  
**Monolithic Low Power CMOS Design**

## APPLICATIONS

**Signal Processing Systems**  
**Multichannel Data Acquisition Systems**  
**Automatic Test Equipment**  
**Medical and Analytical Instrumentation**  
**Event Analysis**  
**DAC Deglitching**

## FUNCTIONAL BLOCK DIAGRAM



## GENERAL DESCRIPTION

The SMP04 is a monolithic quad sample-and-hold; it has four internal precision buffer amplifiers and internal hold capacitors. It is manufactured in ADI's advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate and fast acquisition time required by data acquisition and signal processing systems. The device can acquire an 8-bit input signal to  $\pm 1/2$  LSB in less than seven microseconds. The SMP04 can operate from single or dual power supplies with TTL/CMOS logic compatibility. Its output swing includes the negative supply.

The SMP04 is ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more can be used with a single or multiple DACs to provide multiple setpoints within a system.

The SMP04 offers significant cost and size reduction over equivalent module or discrete designs. It is available in a 16-pin hermetic or plastic DIP and surface mount SOIC packages. It is specified over the extended industrial temperature range of 0°C to +85°C.

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# SMP04- SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

(@  $V_{DD} = +12.0\text{ V}$ ,  $V_{SS} = \text{DGND} = 0\text{ V}$ ,  $R_L = \text{No Load}$ ,  $T_A = \text{Operating Temperature Range}$  specified in Absolute Maximum Ratings, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error				0.01		%
Buffer Offset Voltage	$V_{OS}$	$V_{IN} = 6\text{ V}$	-10	$\pm 2.5$	+10	mV
Hold Step	$V_{HS}$	$V_{IN} = 6\text{ V}$		1	$\pm 4$	mV
Droop Rate	$\Delta V/\Delta t$	$V_{IN} = 6\text{ V}$ , $T_A = +25^\circ\text{C}$		2	25	mV/s
Output Source Current	$I_{SOURCE}$	$V_{IN} = 6\text{ V}^1$	1.2			mA
Output Sink Current	$I_{SINK}$	$V_{IN} = 6\text{ V}^1$	0.5			mA
Output Voltage Range	OVR	$R_L = 20\text{ k}\Omega$	0.06		10.0	V
		$R_L = 10\text{ k}\Omega$	0.06		9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	$V_{INH}$		2.4			V
Logic Input Low Voltage	$V_{INL}$				0.8	V
Logic Input Current	$I_{IN}$			0.5	1	$\mu\text{A}$
DYNAMIC PERFORMANCE <sup>2</sup>						
Acquisition Time	$t_A$	$T_A = +25^\circ\text{C}$ , 0 V to 10 V Step to 0.1%		7		$\mu\text{s}$
Acquisition Time	$t_A$	$T_A = +25^\circ\text{C}$ , 0 V to 10 V Step to 0.01%		9		$\mu\text{s}$
Hold Mode Settling Time	$t_H$	To 1 mV		1		$\mu\text{s}$
Slew Rate	SR	$R_L = 20\text{ k}\Omega^3$	3	4		V/ $\mu\text{s}$
Capacitive Load Stability	$C_L$	<30% Overshoot		500		pF
Analog Crosstalk		0 V to 10 V Step		-80		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	$10.8\text{ V} \leq V_{DD} \leq 13.2\text{ V}$	60	75		dB
Supply Current	$I_{DD}$			4	7	mA
Power Dissipation	$P_{DIS}$				84	mW

## ELECTRICAL CHARACTERISTICS

(@  $V_{DD} = +5.0\text{ V}$ ,  $V_{SS} = -5.0\text{ V}$ ,  $\text{DGND} = 0.0\text{ V}$ ,  $R_L = \text{No Load}$ ,  $T_A = \text{Operating Temperature Range}$  specified in Absolute Maximum Ratings, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error				0.01		%
Buffer Offset Voltage	$V_{OS}$	$V_{IN} = 0\text{ V}$	-10	$\pm 2.5$	+10	mV
Hold Step	$V_{HS}$	$V_{IN} = 0\text{ V}$		-1	$\pm 4$	mV
Droop Rate	$\Delta V/\Delta t$	$V_{IN} = 0\text{ V}$ , $T_A = +25^\circ\text{C}$		2	25	mV/s
Output Resistance	$R_{OUT}$			1		$\Omega$
Output Source Current	$I_{SOURCE}$	$V_{IN} = 0\text{ V}^1$	1.2			mA
Output Sink Current	$I_{SINK}$	$V_{IN} = 0\text{ V}^1$	0.5			mA
Output Voltage Range	OVR	$R_L = 20\text{ k}\Omega$	-3.0		+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	$V_{INH}$		2.4			V
Logic Input Low Voltage	$V_{INL}$				0.8	V
Logic Input Current	$I_{IN}$			0.5	1	$\mu\text{A}$
DYNAMIC PERFORMANCE <sup>2</sup>						
Acquisition Time	$t_A$	-3 V to +3 V Step to 0.1%		7		$\mu\text{s}$
Acquisition Time	$t_A$	-3 V to +3 V Step to 0.01%		9		$\mu\text{s}$
Hold Mode Settling Time	$t_H$	To 1 mV		1		$\mu\text{s}$
Slew Rate	SR	$R_L = 20\text{ k}\Omega^4$		3		V/ $\mu\text{s}$
Capacitive Load Stability	$C_L$	<30% Overshoot	500			pF
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	$\pm 5\text{ V} \leq V_{DD} \leq \pm 6\text{ V}$	60	75		dB
Supply Current	$I_{DD}$			3.5	5.5	mA
Power Dissipation	$P_{DIS}$				55	mW

### NOTES

<sup>1</sup>Outputs are capable of sinking and sourcing over 20 mA but linearity and offset are guaranteed at specified load levels.

<sup>2</sup>All input control signals are specified with  $t_R = t_F = 5\text{ ns}$  (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

<sup>3</sup>Slew rate is measured in the sample mode with a 0 V to 10 V step from 20% to 80%.

<sup>4</sup>Slew rate is measured in the sample mode with a -3 V to +3 V step from 20% to 80%.

Specifications are subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

( $T_A = +25^\circ\text{C}$  unless otherwise noted)

$V_{DD}$ to DGND	-0.3 V, 17 V
$V_{DD}$ to $V_{SS}$	-0.7 V, 17 V
$V_{LOGIC}$ to DGND	-0.3 V, $V_{DD}$
$V_{IN}$ to DGND	$V_{SS}$ , $V_{DD}$
$V_{OUT}$ to DGND	$V_{SS}$ , $V_{DD}$
Analog Output Current (Not Short-Circuit Protected)	$\pm 20\text{ mA}$
Digital Input Voltage to DGND	-0.3 V, $V_{DD} + 0.3\text{ V}$
Operating Temperature Range	
EQ, EP, ES	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
AQ	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

Package Type	$\theta_{JA}^*$	$\theta_{JC}$	Units
16-Pin Cerdip (Q)	94	12	$^\circ\text{C/W}$
16-Pin Plastic DIP (P)	76	33	$^\circ\text{C/W}$
16-Pin SO (S)	92	27	$^\circ\text{C/W}$

\* $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for cerdip and plastic DIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

## CAUTION

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and function operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
- Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
- Remove power before inserting or removing units from their sockets.

## PIN CONNECTIONS

16-Pin Cerdip

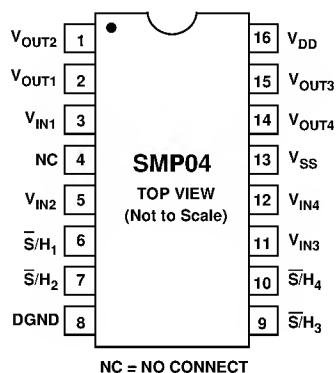
(Q Suffix)

16-Pin Plastic DIP

(P Suffix)

16-Pin SO

(S Suffix)



## ORDERING GUIDE

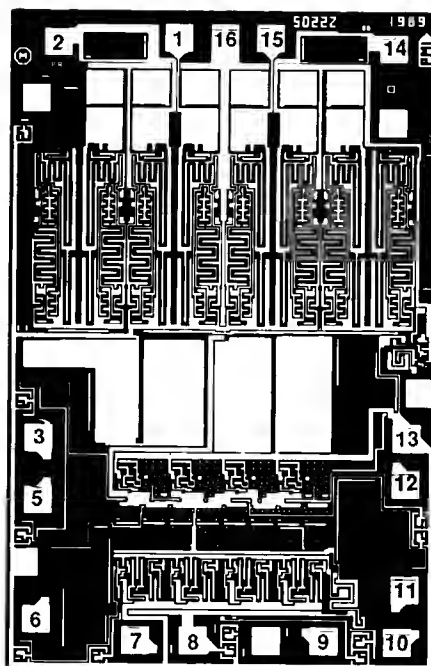
Model	Temperature Range	Package Description	Package Option
SM P04EQ	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	Cerdip-16	Q-16
SM P04EP	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	PDIP-16	N-16
SM P04ES	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	SO-16	R-16A

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SMP04 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# SMP04



*Dice Characteristics*

## WAFER TEST LIMITS (@ $V_{DD} = +12\text{ V}$ , $V_{SS} = \text{DGND} = 0\text{ V}$ , $R_L = \text{No Load}$ , $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	SMP04G Limits	Units
Buffer Offset Voltage	V <sub>OS</sub>	V <sub>IN</sub> = +6 V	±10	mV max
H old Step	V <sub>HS</sub>	V <sub>IN</sub> = +6 V	±4	mV max
D roop Rate	ΔV/Δt	V <sub>IN</sub> = +6 V	25	mV/s max
Output Source Current	I <sub>SOURCE</sub>	V <sub>IN</sub> = +6 V	1.2	mA min
Output Sink Current	I <sub>SINK</sub>	V <sub>IN</sub> = +6 V	0.5	mA min
Output Voltage Range	OVR	R <sub>L</sub> = 20 kΩ	0.06/10.0	V max/min
		R <sub>L</sub> = 10 kΩ	0.06/9.5	V max/min
LOGIC CHARACTERISTICS				
Logic Input High Voltage	V <sub>INH</sub>	V <sub>IN</sub> = 2.4 V	2.4	V min
Logic Input Low Voltage	V <sub>INL</sub>		0.8	V max
Logic Input Current	I <sub>IN</sub>		1	μA max
SUPPLY CHARACTERISTICS				
Power Supply Rejection Ratio	PSRR	10.8 V ≤ V <sub>DD</sub> ≤ 13.2 V	60	dB min
Supply Current	I <sub>DD</sub>		7	mA max
Power Dissipation	P <sub>DIS</sub>		84	mW max

### NOTE

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

# Typical Performance Characteristics- SMP04

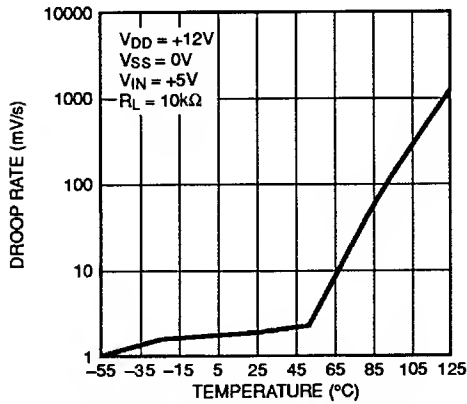


Figure 1. Droop Rate vs. Temperature

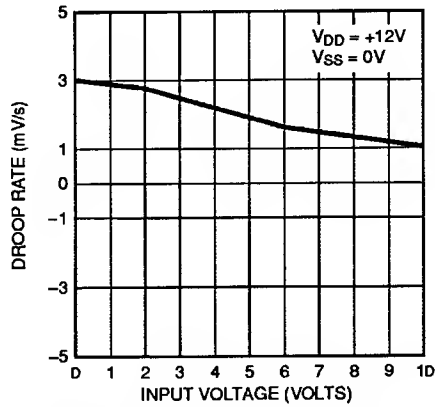


Figure 2. Droop Rate vs. Input Voltage ( $T_A = +25^\circ\text{C}$ )

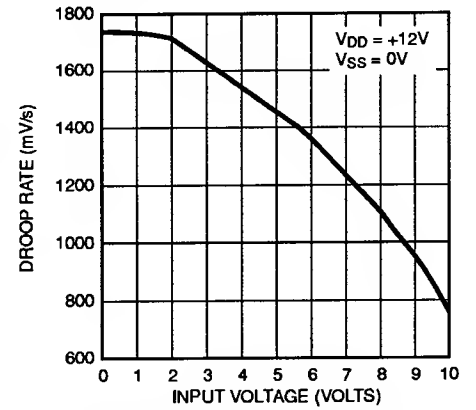


Figure 3. Droop Rate vs. Input Voltage ( $T_A = +125^\circ\text{C}$ )

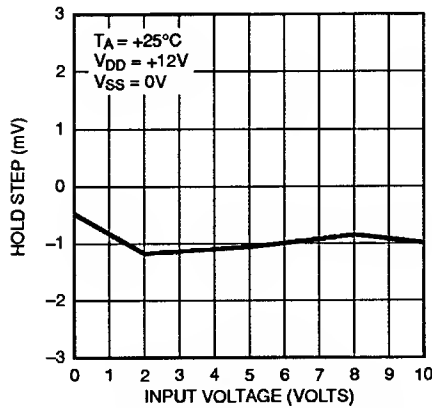


Figure 4. Hold Step vs. Input Voltage

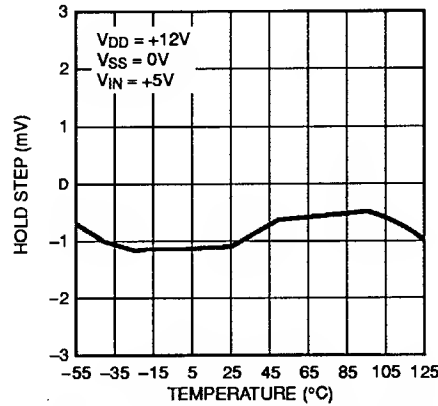


Figure 5. Hold Step vs. Temperature

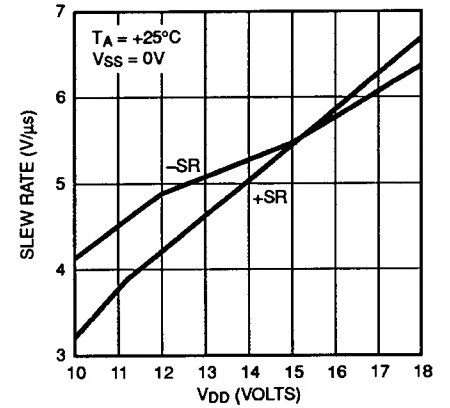


Figure 6. Slew Rate vs.  $V_{DD}$

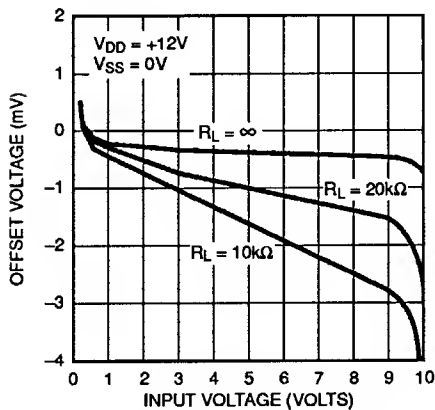


Figure 7. Offset Voltage vs. Input Voltage ( $T_A = +25^\circ\text{C}$ )

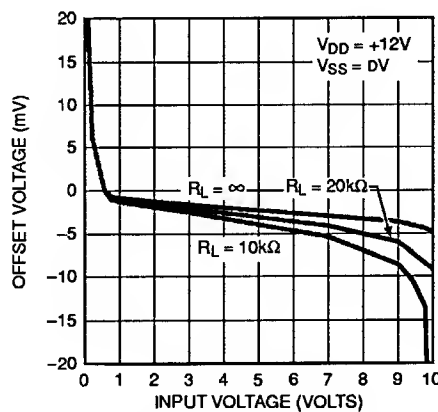


Figure 8. Offset Voltage vs. Input Voltage ( $T_A = +125^\circ\text{C}$ )

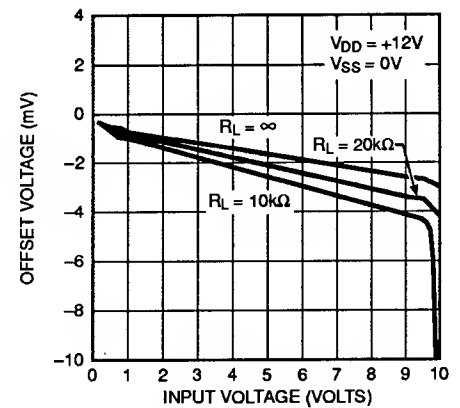


Figure 9. Offset Voltage vs. Input Voltage ( $T_A = -55^\circ\text{C}$ )

# SMP04

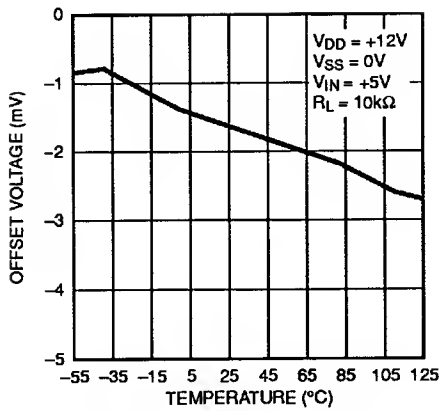


Figure 10. Offset Voltage vs. Temperature

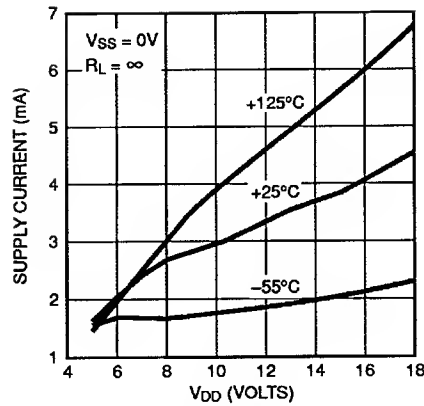


Figure 11. Supply Current vs.  $V_{DD}$

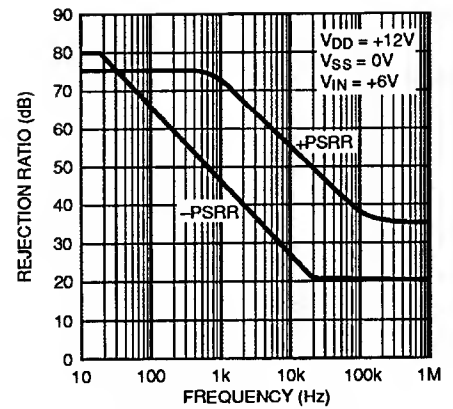


Figure 12. Sample Mode Power Supply Rejection

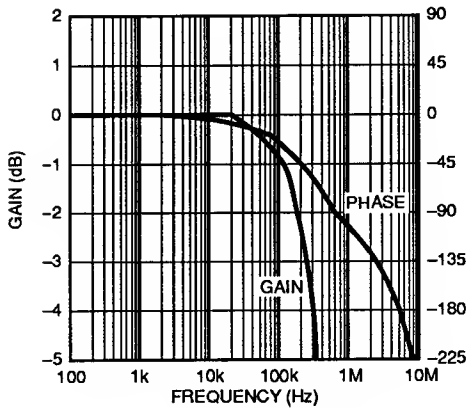


Figure 13. Gain, Phase Shift vs. Frequency

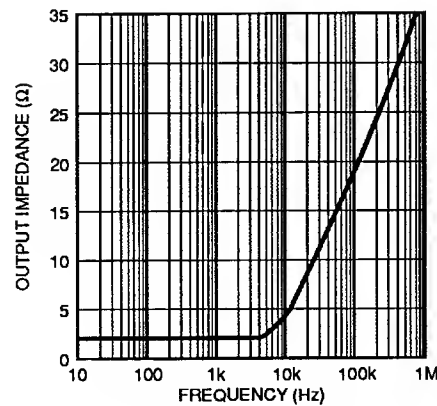


Figure 14. Output Impedance vs. Frequency

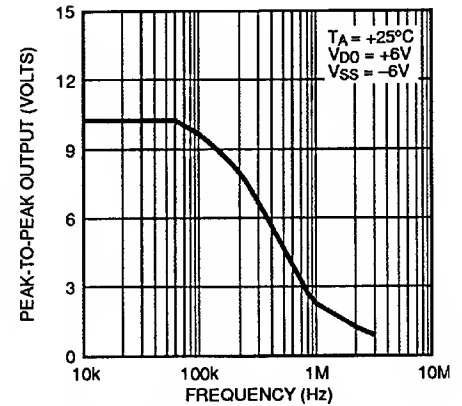


Figure 15. Maximum Output Voltage vs. Frequency

## GENERAL INFORMATION

The SM P04 is a quad sample-and-hold with each track-and-hold having its own input, output, control, and on-chip hold capacitor. The combination of four high performance track-and-hold capacitors on a single chip greatly reduces board space and design time while increasing reliability.

After the device selection, the primary considerations in using track-and-holds are the hold capacitor and layout. The SM P04 eliminates most of these problems by having the hold capacitors internal, eliminating the problems of leakage, feedthrough, guard ring layout and dielectric absorption.

## POWER SUPPLIES

The SM P04 is capable of operating with either single or dual supplies over a voltage range of 7 to 15 volts. Based on the supply voltages chosen,  $V_{DD}$  and  $V_{SS}$  establish the output voltage range, which is:

$$V_{SS} + 0.05 \text{ V} \leq V_{OUT} \leq V_{DD} - 2 \text{ V}$$

Note that several specifications, including acquisition time, offset and output voltage compliance will degrade for a total supply voltage of less than 7 V. Positive supply current is typically 4 mA with the outputs unloaded. The SM P04 has an internally regulated TTL supply so that TTL/CMOS compatibility will be maintained over the full supply range.

**Single Supply Operation Grounding Considerations**—In single supply applications, it is extremely important that the  $V_{SS}$  (negative supply) pin be connected to a clean ground. This is because the hold capacitor is internally tied to  $V_{SS}$ . Any noise or disturbance in the ground will directly couple to the output of the sample-and-hold, degrading the signal-to-noise performance. It is advisable that the analog and digital ground traces on the circuit board be physically separated to reduce digital switching noise from entering the analog circuitry.

**Power Supply Bypassing**—For optimum performance, the  $V_{DD}$  supply pin must also be bypassed with a good quality, high frequency ceramic capacitor. The recommended value is  $0.1\ \mu\text{F}$ . In the case where dual supplies are used,  $V_{SS}$  (negative supply) bypassing is particularly important. Again this is because the internal hold capacitor is tied to  $V_{SS}$ . Good bypassing prevents high frequency noise from entering the sample-and-hold amplifier. A  $0.1\ \mu\text{F}$  ceramic bypass capacitor is generally sufficient. For high noise environments, adding a  $10\ \mu\text{F}$  tantalum capacitor in parallel with the  $0.1\ \mu\text{F}$  provides additional protection.

**Power Supply Sequencing**—It may be advisable to have the  $V_{DD}$  turn on prior to having logic levels on the inputs. The SM P04 has been designed to be resistant to latch-up, but standard precautions should still be taken.

#### OUTPUT BUFFERS (Pins 1, 2, 14, and 15)

The buffer offset specification is  $\pm 10\ \text{mV}$ ; this is less than  $1/2\ \text{LSB}$  of an 8-bit DAC with  $10\ \text{V}$  full scale. Change in offset over the output range is typically  $3\ \text{mV}$ . The hold step is the magnitude of the voltage step caused when switching from sample-to-hold mode. This error is sometimes referred to as the pedestal error or sample-to-hold offset, and is about  $1\ \text{mV}$  with little variation. The droop rate of a held channel is  $2\ \mu\text{V}/\text{ms}$  typical and  $\pm 25\ \mu\text{V}/\text{ms}$  maximum.

The buffers are designed primarily to drive loads connected to ground. The outputs can source more than  $1.2\ \text{mA}$  each, over the full voltage range and maintain specified accuracy. In split supply operation, symmetrical output swings can be obtained by restricting the output range to  $2\ \text{V}$  from either supply.

On-chip SM P04 buffers eliminate potential stability problems associated with external buffers; outputs are stable with capacitive loads up to  $500\ \text{pF}$ . However, since the SM P04's buffer outputs are not short-circuit protected, care should be taken to avoid shorting any output to the supplies or ground.

#### SIGNAL INPUT (Pins 3, 5, 11, and 12)

The signal inputs should be driven from a low impedance voltage source such as the output of an op amp. The op amp should have a high slew rate and fast settling time if the SM P04's fast acquisition time characteristics are to be maintained. As with all CMOS devices, all input voltages should be kept within range of the supply rails ( $V_{SS} \leq V_{IN} \leq V_{DD}$ ) to avoid the possibility of setting up a latch-up condition.

The internal hold capacitance is typically  $60\ \text{pF}$  and the internal switch ON resistance is  $4\ \text{k}\Omega$ .

If single supply operation is desired, op amps such as the OP21, OP80, or OP90 that have input and output voltage compliances including ground, can be used to drive the inputs. Split supplies, such as  $\pm 7.5\ \text{V}$ , can be used with the SM P04 and the above mentioned op amps.

#### APPLICATION TIPS

All unused digital inputs should be connected to logic LOW and the analog inputs connected to analog ground. For connect or driven analog inputs that may become temporarily disconnected, a resistor to  $V_{SS}$  or analog ground should be used with a value ranging from  $0.2\ \text{M}\Omega$  to  $1\ \text{M}\Omega$ .

Do not apply signals to the SM P04 with power off unless the input current's value is limited to less than  $10\ \text{mA}$ .

Track-and-holds are sensitive to layout and physical connections. For the best performance, the SM P04 should not be socketed.

#### FREQUENCY DOMAIN PERFORMANCE

The SM P04 has been characterized in the frequency domain for those applications that require capture of dynamic signals. See Figure 16a for typical  $86.1\ \text{kHz}$  sample rate and an  $8\ \text{kHz}$  input signal. Typically, the SM P04 can sample at rates up to  $85\ \text{kHz}$ . In addition to the maximum sample rate, a minimum sample pulse width will also be acceptable for a given design. Our testing shows a drop in performance as the sample pulse width becomes less than  $4\ \mu\text{s}$ .

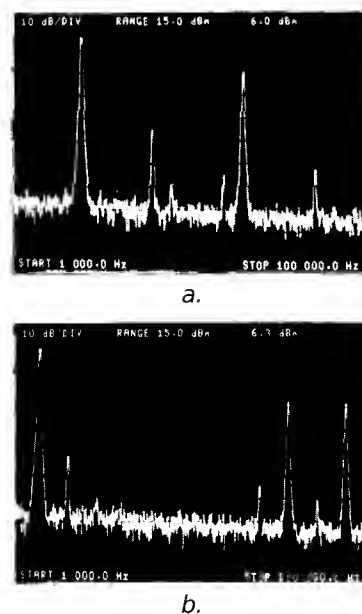


Figure 16. Spectral response at a sampling frequency of  $86\ \text{kHz}$ . Photo (a) shows a  $20\ \text{kHz}$  carrier frequency, and photo (b) shows an  $8\ \text{kHz}$  frequency.

# SMP04

**Optimizing Dynamic Performance of the SMP04**—Various operating parameters such as input voltage amplitude, sampling pulse width and, as mentioned before, supply bypassing and grounding all have an effect on the signal-to-noise ratio. Table I shows the SNR versus input level for the SM P04.

Distortion of the SM P04 is reduced by increasing the supply voltage. This has the effect of increasing the positive slew rate. Table II shows data taken at 12.3 kHz sample rate and 2 kHz input frequency. Total harmonic distortion is dominated by the second and third harmonics.

Table III shows the effect of sampling pulse width on the SNR of the SM P04. The recommended operating pulse width should be a minimum of 5  $\mu$ s to achieve a good balance between acquisition time and SNR for the 1.4 V p-p signal shown. For larger swings the pulse width will need to be larger to account for the time required for the signal to slew the additional voltage. This could be used as a method of measuring acquisition time indirectly.

**Table I. SNR vs.  $V_{IN}$**

Input Voltage (V p-p)	SNR (dB)
1	-61
2	-53
3	-50
4	-47
5	-45
6	-44

Conditions:  $V_S = \pm 6$  V,  $f_S = 14.4$  kHz,  $f_{IN} = 1.8$  kHz,  $t_{PW} = 10$   $\mu$ s.

**Table II. SNR vs. Supply Voltage**

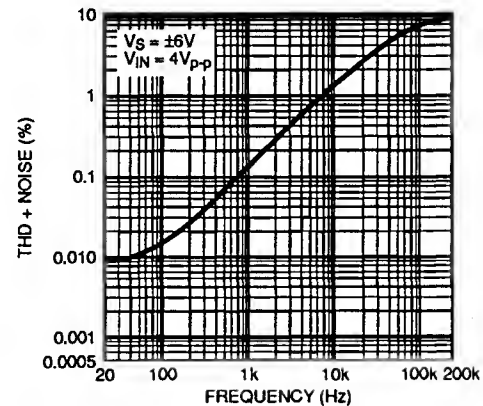
Supply Voltage (V)	2nd (dB)	3rd (dB)
10	-49	-62
12	-55	-71
14	-60	-80
15	-62	<-80
16	-63	<-83
17	-65	<-85

**Table III. SNR vs. Sample Pulse Width**

Sample Pulse Width ( $\mu$ s)	SNR (dB)
1	-37
2	-44
3	-50
4	-54
5	-54.9
6	-55
7	-55.3

Conditions:  $V_S = \pm 6$  V,  $V_{IN} = 1.4$  V p-p,  $f_S = 14.4$  kHz,  $f_{IN} = 1.8$  kHz.

**Sample-Mode Distortion Characteristics**—Although designed as a sample-and-hold, the SM P04 may be used as a straight buffer amplifier by configuring it in a continuous sample mode. This is done by connecting the  $\bar{S}/H$  control pin to a logic LOW. Its buffer bandwidth is primarily limited by the distortion content as the signal frequency increases. Figure 17 shows the distortion characteristics of the SM P04 versus frequency. It maintains less than 1% total harmonic distortion over a voiceband of 8 kHz.



*Figure 17. THD+N vs. Frequency*



**Sampled Data Dynamic Performance**—In continuous sampled data applications such as voice digitization or communication circuits, it is important to analyze the spectral response of a sample-and-hold. Figures 16a and 16b show the SMP04 sampling at a frequency of 86 kHz with a 1.4 V p-p pure sine wave input of 20 kHz and 8 kHz respectively. The photos include the sampling carrier frequency as well as its multiplying frequencies. In the case of the 20 kHz carrier frequency, the second harmonic measures 41 dB down from the fundamental, because the second is dominant,

the signal-to-noise ratio is -40.9 dB. The 8 kHz case produces an improved S/N performance of -48 dB.

In the V.32 and V.33 modem environment, where a 1.8 kHz carrier signal frequency is applied to the SMP04, Figure 18 compares the spectral responses of the SMP04 under three different sampling frequencies of 14.4 kHz, 9.6 kHz and 7.2 kHz. The signal-to-noise ratios measure to be 58.2 dB, 59.3 dB and 60 dB respectively.

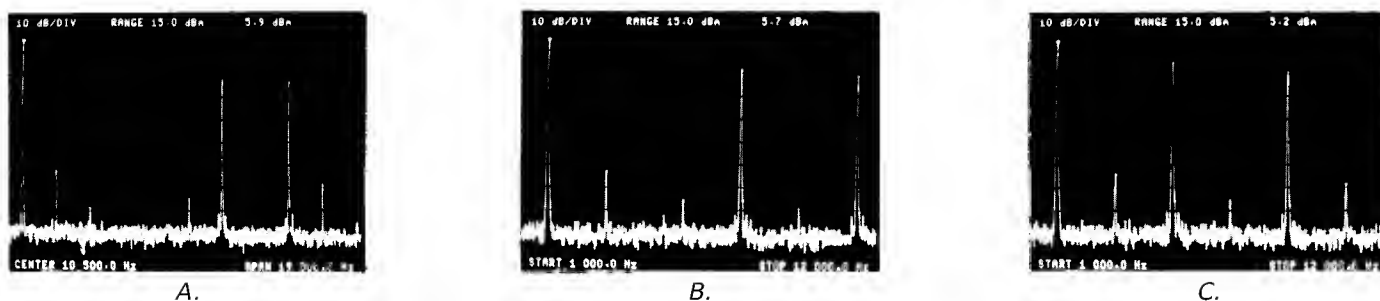


Figure 18. SMP04 spectral response with a 1.8 kHz carrier frequency. (a) shows the sampling frequency at 14.4 kHz; it exhibits a S/N ratio of 58.2 dB. (b) shows a 59.3 dB S/N at a sampling frequency of 8.6 kHz. (c) shows a 60 dB S/N at 7.2 kHz.

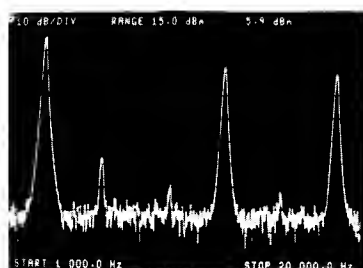


Figure 19. SMP04 spectral response with an input carrier frequency of 3 kHz and the sampling frequency of 15.7 kHz.

Figure 19 depicts SMP04's spectral response operating with voice frequency of 3 kHz sampling at a 15.7 kHz rate. Under this condition, the signal-to-noise measures 53 dB.

**SMP04**

## APPLICATIONS

### MULTIPLEXED QUAD DAC (Figure 20)

The SM P04 can be used to demultiplex a single DAC converter's output into four separate analog outputs. The circuit is greatly simplified by using a voltage output DAC such as the DAC8228. To minimize output voltage perturbation, 5  $\mu$ s should be allowed to settle to its final voltage before a sample signal is asserted. Each sample-and-hold amplifier must be refreshed every second or less in order to assure the droop does not exceed 10 mV or 1/2 LSB.

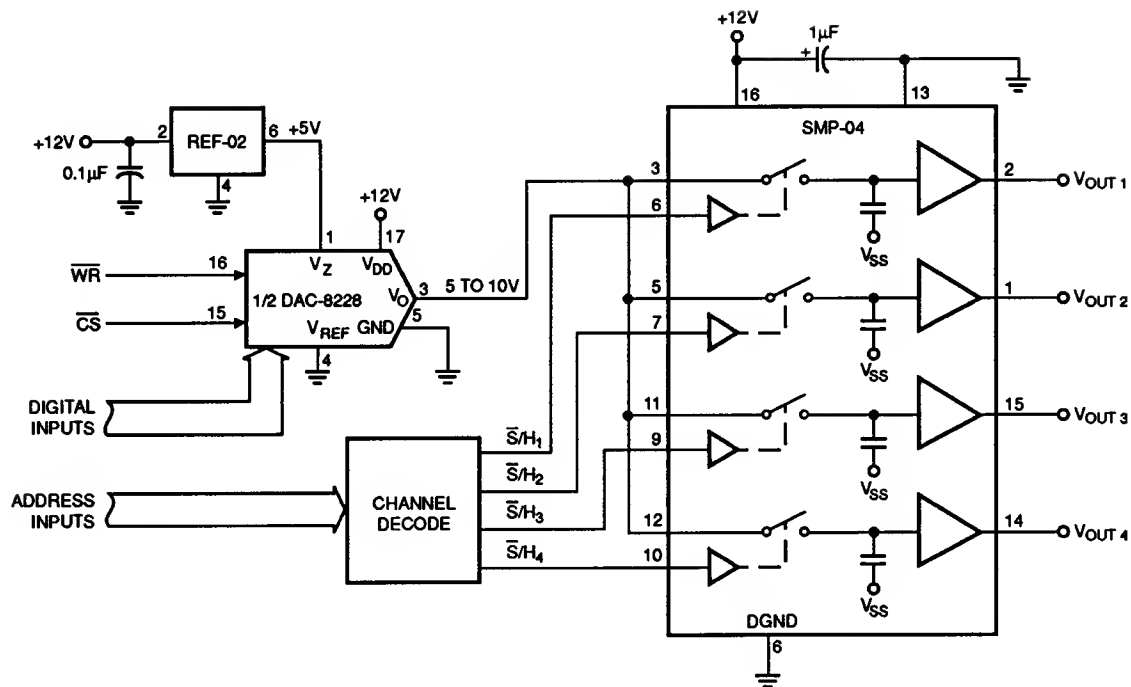


Figure 20. Multiplexed Quad DAC

### POSITIVE AND NEGATIVE PEAK DETECTOR WITH HOLD CONTROL (Figure 21)

In this application the top amplifier (Amplifier A) is the positive peak detector and the bottom amplifier (Amplifier B) is the negative peak detector. Operation can be analyzed as follows: Assume that the  $\overline{\text{S/H}}$  switch is closed. As a positive increasing voltage is applied to  $A_{IN}$ ,  $D_2$  turns on, and  $D_1$  turns off, closing the feedback loop around Amplifier A and the SMP04, causing the output to track the input. Conversely, in the negative peak detector circuit at the bottom,  $D_4$  turns off and  $D_3$  turns on, holding the last most negative input voltage on the SMP04. This voltage is buffered to the  $V_{O(NEG)}$  output.

As  $V_{IN}$  falls in voltage the above conditions reverse, causing the most positive peak voltage to be held at  $V_{O(POS)}$  output. This voltage will be held until the input has a more positive voltage than the previously held peak voltage, or a reset condition is applied.

An optional HOLD control can be used by applying a logic HIGH to the  $\overline{\text{PD/H}}$  inputs. This HOLD mode further reduces leakage current through the reverse-biased diodes ( $D_2$  and  $D_4$ ) during peak hold.

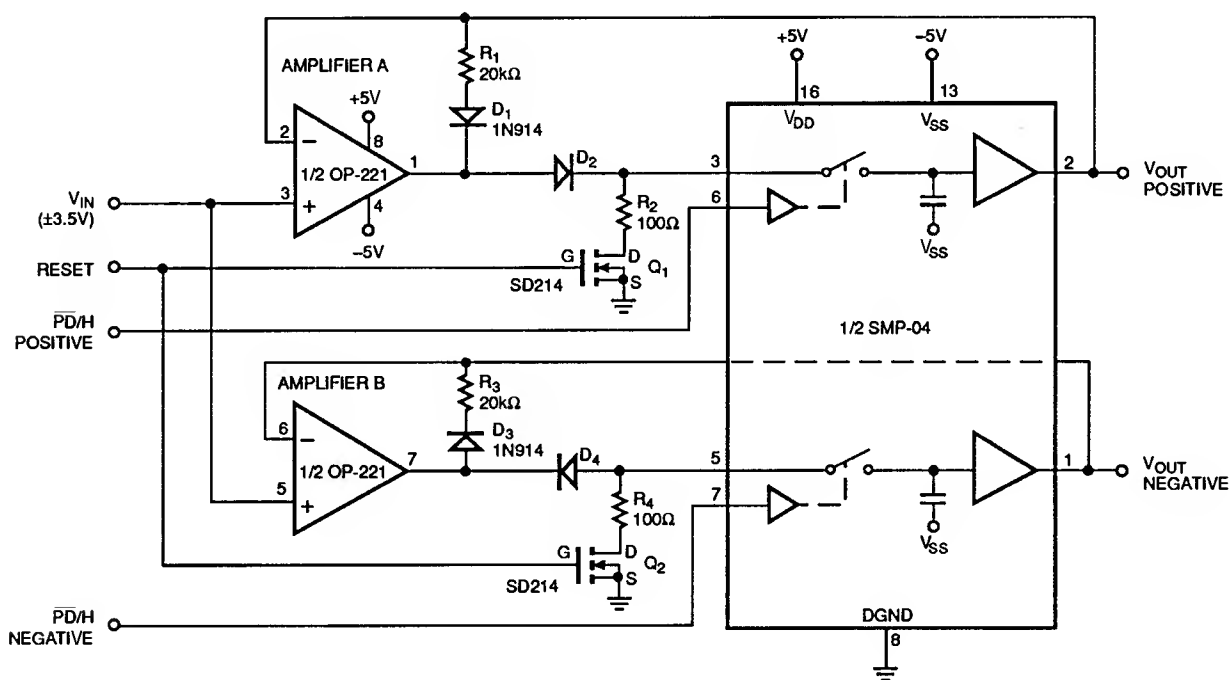


Figure 21. Positive and Negative Peak Detector with Hold Control

# SMP04

## GAIN OF 10 SAMPLE-AND-HOLD (Figure 22)

This application places the SMP04 in a feedback loop of an amplifier. Because the SMP04 has no sign inversion and the amplifier has very high open-loop gain, the gain of the circuit is set by the ratio of the sum of the source and feedback resistances

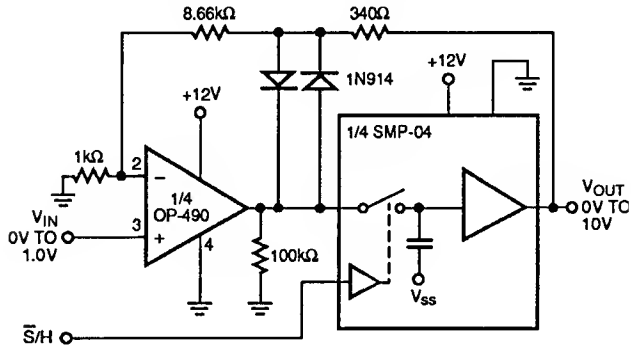


Figure 22. Gain of 10 Sample-and-Hold Amplifier

to the source resistance. When a logic LOW is applied to the  $\overline{S/H}$  control input, the loop is closed around the OP490, yield-

ing a gain of 10 (in the example shown) amplifier. When the  $\overline{S/H}$  control goes HIGH, the loop opens and the SMP04 holds the last sampled voltage. The loop remains open and the output is unaffected by the input until a logic LOW is reapplied to the  $\overline{S/H}$  control. The pair of back-to-back diodes from the output of the op amp to the output of the track-and-hold prevents the op amp from saturating when the track-and-hold is in the hold mode and the loop is open.

## SAMPLE AND DIFFERENCE AMPLIFIER (Figure 23)

This circuit uses two sample-and-holds to measure the voltage difference of a signal between two time points,  $t_1$  and  $t_2$ . The sampled voltages are fed into the differential inputs of the AMP02 instrumentation amplifier. A single resistor  $R_G$  sets the gain of this instrumentation amplifier. Using two of the SMP04s in this application has the advantage of matched sample-and-hold performance, since they are both on the same chip.

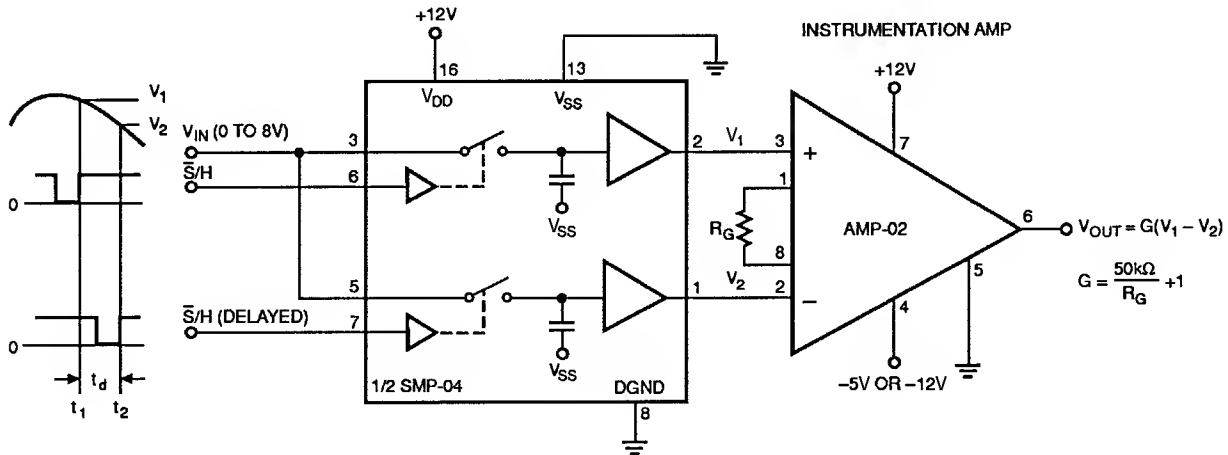


Figure 23. Time Delta Sample-and-Difference Measurement

### SINGLE SUPPLY, SAMPLING, INSTRUMENTATION AMPLIFIER (Figure 24)

This application again uses two channels of the SM P04 and an instrumentation amplifier to provide a sampled difference signal. The sample-and-hold signals in this circuit are tied together to sample at the same point in time. The other two parts of the SM P04 are used as amplifiers by grounding their control lines so that they are always sampling. One section is used to drive a guard to the common-mode voltage and the other to generate a +6 V reference to serve as an offset for single supply operation.

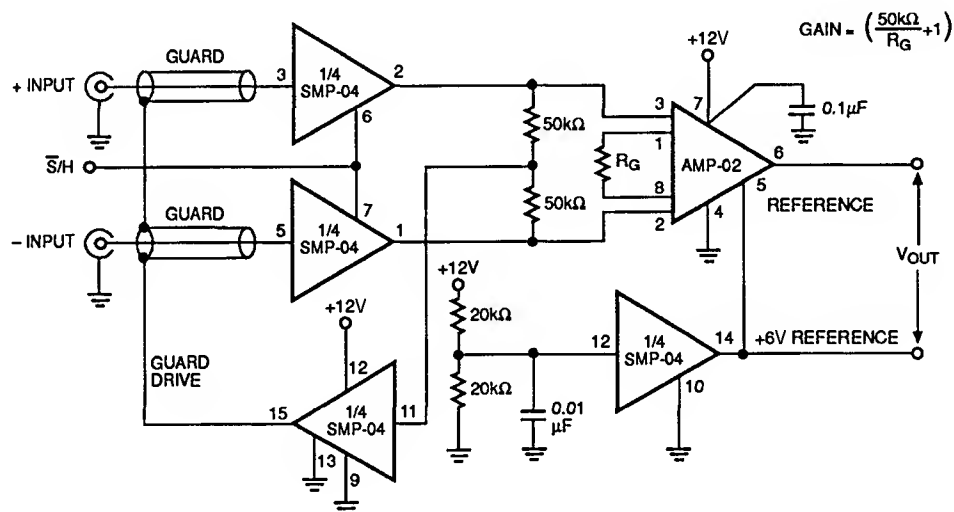


Figure 24. +12 V Single Supply Sampling Instrumentation Amplifier with Guard Drive

# SMP04

## D/A CONVERTER DEGLITCHER

Most D/A converters output an appreciable amount of glitch energy during a transition from one code to another. The glitch amplitude can range from several millivolts to hundreds of millivolts. This may become unacceptable in many applications. By selectively delaying the DAC's output transition, the SMP04 can be used to smooth the output waveform. Figure 25 shows the schematic diagram of such a deglitcher circuit. Two simple logic gates (an OR and a NAND gate) provide the proper timing sequence for the DAC  $\overline{WR}$  strobe and the  $\overline{S}/H$  control signal to the SMP04. In this example a linear ramp signal is generated by feeding the most significant 8-bits of the 10-bit binary counter to the DAC. The two least significant bits are used to produce the delayed  $\overline{WR}$  strobe and the  $\overline{S}/H$  control signals. Referring to Figure 26a, new data to the DAC

input is set up at the  $\overline{S}/H$ 's falling edge, but the DAC output does not change yet until a  $\overline{WR}$  strobe goes active. During this period, the SMP04 is in a sample mode whose output tracks the DAC output. When  $\overline{S}/H$  goes HIGH, the current DAC output voltage is held by the SMP04. After 1.2  $\mu s$  settling, the  $\overline{WR}$  strobe goes LOW to allow the DAC output to change. Any glitch that occurs at the DAC output is effectively blocked by the SMP04. As soon as the  $\overline{WR}$  strobe goes HIGH, the digital data is latched; at the same time the  $\overline{S}/H$  goes LOW, allowing the SMP04 to track to the new DAC output voltage.

Figure 27b shows the deglitching operation. The top trace shows the DAC output during a transition, while the bottom trace shows the deglitched output of the SMP04.

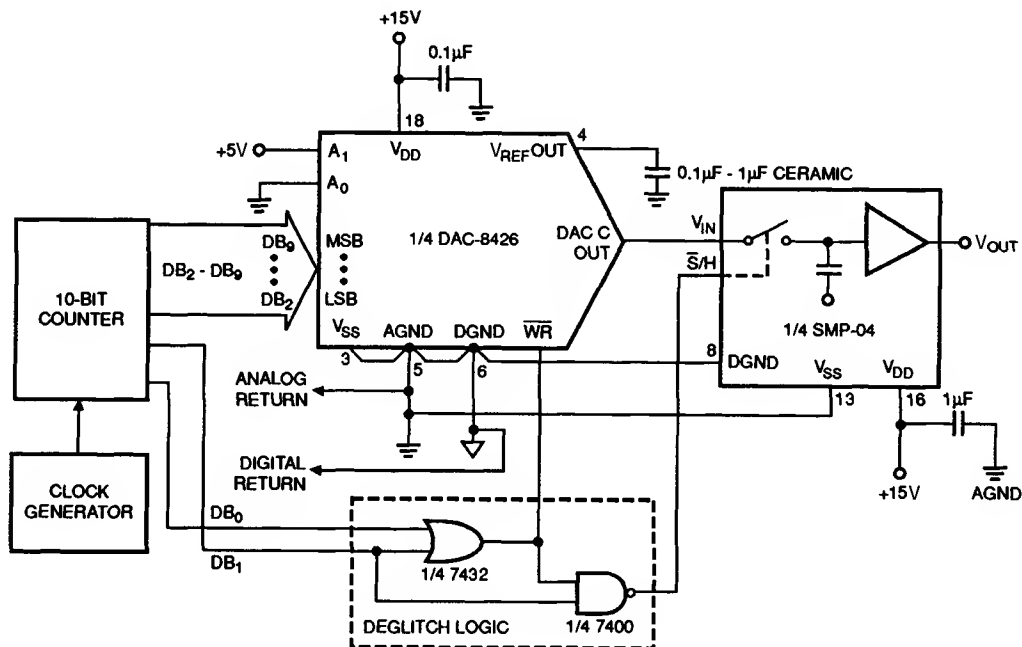
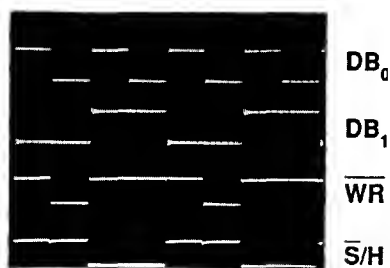
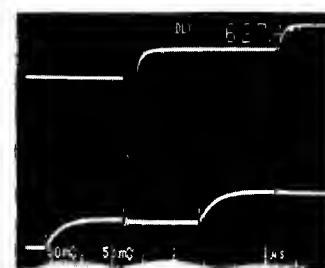


Figure 25. DAC Deglitcher



a.



b.

Figure 26. (a) shows the logic timing of the deglitcher. The top two traces are the two least significant bits,  $DB_0$  and  $DB_1$ , respectively. These are used to generate the  $\overline{WR}$  and  $\overline{S}/H$  signals which are shown in the bottom two traces. (b) shows the typical glitch amplitude of a DAC (top trace) and the deglitched output of the AMP04 (bottom trace).

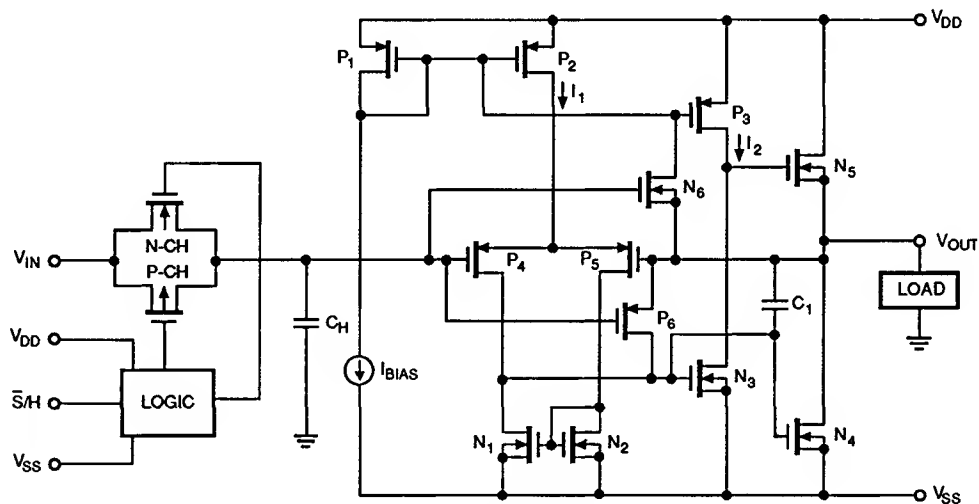


Figure 27. Simplified Schematic

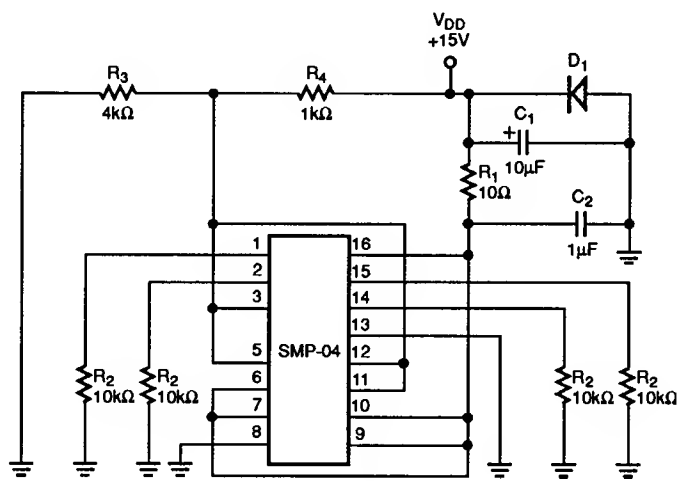
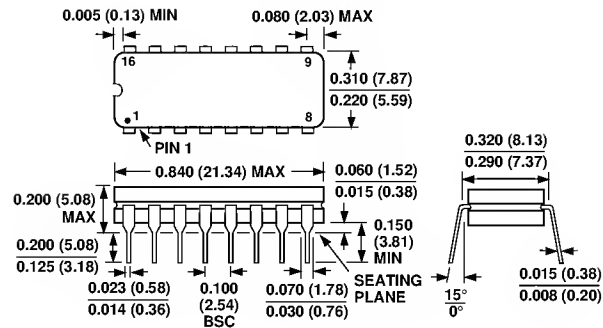
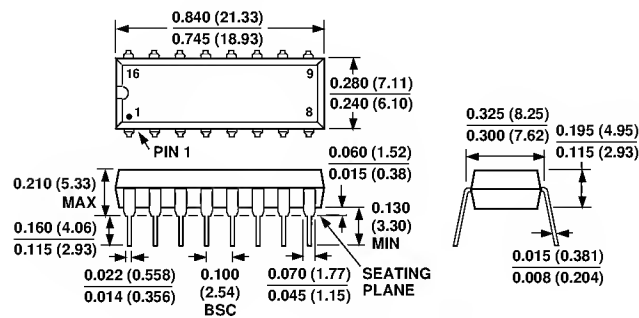


Figure 28. Burn-In Circuit

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**16-Pin Cerdip  
(Q-16 Suffix)****16-Pin Plastic DIP  
(N-16 Suffix)****16-Pin SO  
(R-16A Suffix)**